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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary	Application No. 08/229,526	Applicant(s) Peters et al.
	Examiner St. John Courtenay III	Group Art Unit 2316

☒ Responsive to communication(s) filed on *Jun 17, 1996* .

☒ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *3* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) *1-28* is/are pending in the application.

Of the above, claim(s) _____ is/are withdrawn from consideration.

☒ Claim(s) *8, 9, 22, and 23* is/are allowed.

☒ Claim(s) *1-7, 10-21, and 24-28* is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☒ The proposed drawing correction, filed on *Jun 17, 1996* is ☒approved ☐disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____ .

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____ .

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☐ Notice of References Cited, PTO-892

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). 11

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

Response to Amendment - Final Rejection

This final rejection is in response to Amendment A of Application **08/229,526.** This application was filed in the United States of America on 4-19-94. Amendment A was received on 6-17-96. This application is a RULE 47 continuation of U.S. application Ser. No. 08/203/531 (filed Feb. 28, 1994) which is copending.

Response to Applicant's Arguments:

Applicant argues: *"that a thread cannot be both a segment and an independent sub-event, as claimed. As recited in claim 1, a segment comprises a plurality of discrete events, each discrete event comprising a plurality of independent sub-events."*

In response, the Examiner notes that claim 1 explicitly recites *"each segment comprising a sequence of at least one discrete event to be processed.* Therefore, as claimed, a single discrete event meets the limitations associated with a "segment". The Examiner acknowledges that a clear distinction in the art exists between an event and a thread, although processes and/or threads are used to handle or process events in the cited combination of references. A *segment* is first recited in the claim to be at least one *event* to be processed, then the segments are executed concurrently in the following step of claim 1, e.g., *"initiating each of said plurality of segments to execute concurrently on said at least one processor."* As is well-known, only code can be executed by a computer system. An event per se is not executable, hence the scope of Applicant's claimed "segment" appears to be broader than an event taken alone. Since Applicant also recites a "segment" as being *executable* it is reasonable to interpret the scope of the "segment" to also encompass the code, process, or thread associated with the processing of an event. As is well-known, an "event" is generally construed in the art to be an occurrence which requires

processing, e.g., a mouse movement, a keypress, failure events, as disclosed by Record [col. 1]. Applicant claims a "segment" is comprised of "at least one event" and also claims a segment that is executable. Accordingly, the Examiner is interpreting the scope of the recited "segment" to include a discrete event (including sub-events) and the code, process(es), or thread(s) that process or handle the discrete event.

Applicant argues that *"there is no suggestion from Spix that any of the events are organized in segments or that there are discrete events comprising independent sub-events which are processed sequentially within each discrete event or that the discrete events are processed sequentially within each segment."*

In response the Examiner notes that Applicant's arguments are directed primarily to the perceived differences between the claimed invention and the cited Spix reference taken alone, rather than in combination. The Examiner agrees that the Spix reference taken alone fails to teach all aspects of the claimed invention, however, when the Spix and Record references [and Hillis] are considered as an obvious combination, they do teach the claimed invention. Applicant cannot show nonobviousness by attacking the references individually where, as here, the rejection is based on a combination of references. See *in re Keller, 208 USPQ 871 (CCPA 1981).* Record teaches events and related "sub-events" that are processed or handled in a sequential manner: *"A program can specify interest in a combination of events of the same or different types and if the propagation mode is selected, each event handler in a sequence which receives notification of an event can decide to propagate any number or none of the event signals of interest"* [col. 3, lines 12 - 18].

Applicant argues that *"priority schemes are not sequential."* In response, the Examiner notes that processes or threads executed in a particular priority are still executed sequentially in the order determined by their priority.

In response to Applicant's argument that there is no suggestion to combine the references, the Examiner recognizes that references cannot be arbitrarily combined and that there must be some reason why one skilled in the art would be motivated to make the proposed combination of primary and secondary references. In re Nomiya, 184 USPQ 607 (CCPA 1975). However, there is no requirement that a motivation to make the modification be expressly articulated. The test for combining references is what the combination of disclosures taken as a whole would suggest to one of ordinary skill in the art. In re McLaughlin, 170 USPQ 209 (CCPA 1971) references are evaluated by what they suggest to one versed in the art, rather than by their specific disclosures. In re Bozek, 163 USPQ 545 (CCPA) 1969. In this case, the combination of Spix and Record does produce the required results, as discussed above. The Unix Kernel [fig. 22], the Mach operating system [col. 5], and other operating system environments disclosed by Spix all inherently possess event handling capabilities, as necessary to process disk file I/O, keyboard I/O, printer I/O, etc. Spix explicitly discloses System V file management [col. 31]. Record discloses a system of event handling. Record expliclity discloses in the background of the invention a prior art IBM System/38 operating system and its method of managing events. The use of IBM equipment with superior processing power to manage bill processing and business accounting applications is well-known, if not legendary, e.g, *"International Business Machines"*. Hence, the Examiner maintains that the cited combination of Spix, Record, and Hillis would have been obvious to one of ordinary skill at the time the invention was made.

In response to Applicant's argument that the Examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any

judgement on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. *In re McLaughlin*, 443 F.2d 1392; 170 USPQ 209 (CCPA 1971).

Applicant is reminded that claimed subject matter, not the specification is the measure of the invention. Limitations in the specification cannot be read into the claims for the purpose of avoiding the prior art. See In re Self, 213 USPQ 1,5 (CCPA 1982); In re Priest, 199 USPQ 11, 15 (CCPA 1978). The recited element *"segment"* is clearly subject to a broad interpretation, as detailed above.

Applicant's arguments, filed 6-17-96, have been fully considered but they are not deemed to be persuasive. For the reasons detailed above, all rejections set forth in the previous office action under ***35 U.S.C. 103*** are maintained:

Claim Rejections - 35 U.S.C. § 103

The following is a quotation of 35 U.S.C. § 103 which forms the basis for all obviousness rejections set forth in this Office action:

> *A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.*

Subject matter developed by another person, which qualifies as prior art only under subsection (f) or (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

Claims 1, 4 - 7, 10 - 15, 18 - 21, and 24 - 26 are rejected under 35 U.S.C. § 103 as being unpatentable over Spix et al. (U.S. Patent 5,179,702, issued Jan. 12, 1993) in view of Record et al. (U.S. Patent 5,305,454, issued Apr. 19, 1994, filed Aug. 12, 1991).

As per independent claims 1 and 14:

Spix et al. disclose the invention substantially as claimed, as discussed below: Spix teaches a method for processing a plurality of processes (i.e., "events") in a processing system having at least one processor. Each discrete process (i.e., "event") is comprised of one or more threads (i.e., a plurality of "segments"). Spix teaches an enhanced software architecture which is an improvement over the Dynix operating system implemented by Sequent Computer Systems, as explicitly described in col. 6, lines 7 - 10. This is a symmetrical multiprocessing (SMP) architecture similar to the Sequent Computer system described on page 6 of Applicant's specification [models S2000/450, S2000/750]. Spix teaches that a plurality of segments (i.e., "process queues") are initiated to execute concurrently on at least one processor [col. 9, lines 10 - 15]. Spix teaches that each independent "sub-event" (i.e., "thread") is processed sequentially as determined by priority [col. 9, lines 19 - 23]. It is inherent that the results of the processing are stored. Spix teaches a highly parallel multi processor system having multiple

tightly-coupled processors that share a common memory which stores "discrete events" (i.e., processes and/or threads).

However, ***Spix*** does not explicitly disclose the processing of a plurality of discrete "events".

Record et al. disclose the processing of a plurality of discrete "events" in the analogous field of endeavor of event handling for the purpose of providing a system which efficiently receives sequential notification of an occurrence of an event [abstract].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to improve upon the multi processor scheduler as taught by **Spix** by implementing the processing of a plurality of discrete "events" [event handling] because it would provide **Spix's** system with the enhanced capability of efficiently receiving sequential notification of an occurrence of an event.

As per claim 4:
Record teaches the monitoring of events (i.e. "segments") [figs. 13, 17]. Record teaches the detection of a failure event [col. 2, lines 63 - 68]. Record teaches the dynamic disabling of an event monitor [col. 2, line 2].

As per claim 5:
Record teaches the dynamic enabling (i.e., re-initializing) and disabling of an event monitor [col. 2, line 2].

As per claim 6:

Record teaches a hierarchy of related event handlers including first (i.e., an "individual event") a second event (i.e., a "master event), and a third event (i.e., a "child event") [abstract].

As per claim 7:

Spix teaches the determination of a number of processors designated for processing [col. 9, lines 30 - 45]. Spix teaches that a user may completely control and tune the performance of multithreaded programs (i.e., a "user override" capability) [col. 12, lines 1 - 5]. Record teaches the determination of the number of events to be processed as a hierarchy of first, second, third, ... nth related event handlers [abstract]. Spix teaches a "segment" or queue of requests to be processed [fig. 4a].

As per claim 10:

Spix teaches a plurality of secondary storage units which store the processing results [fig. 2].

As per claim 11:

Spix teaches an enhanced software architecture which is an improvement over the Dynix operating system implemented by Sequent Computer Systems, as explicitly described in col. 6, lines 7 - 10. This is a symmetrical multiprocessing (SMP) architecture similar to the Sequent Computer system described on page 6 of Applicant's specification [models S2000/450, S2000/750].

As per claim 15:

Spix teaches a plurality of processors sharing a single copy of an operating system with each of the processors configured to execute a single process at any one time and each of the processors having read and write access to a least one common memory [abstract, col. 6, lines 7 - 10, col. 7, lines 46 - 59].

As per claim 18:
Record teaches the monitoring of events (i.e. "segments") [figs. 13, 17]. Record teaches the detection of a failure event [col. 2, lines 63 - 68]. Record teaches the dynamic disabling of an event monitor [col. 2, line 2].

As per claim 19:
Record teaches the dynamic enabling (i.e., re-initializing) and disabling of an event monitor [col. 2, line 2].

As per claim 20:
Record teaches a hierarchy of related event handlers including first (i.e., an "individual event") a second event (i.e., a "master event), and a third event (i.e., a "child event") [abstract].

As per claim 21:
Spix teaches the determination of a number of processors designated for processing [col. 9, lines 30 - 45]. Spix teaches that a user may completely control and tune the performance of multithreaded programs (i.e., a "user override" capability) [col. 12, lines 1 - 5]. Record teaches the determination of the number of events to be processed as a hierarchy of first, second, third, ... nth related event handlers [abstract]. Spix teaches a "segment" or queue of requests to be processed [fig. 4a]. Spix teaches work segments that are distributed among the available processors [col. 9, lines 64-65].

As per claim 24:
Spix teaches an enhanced software architecture which is an improvement over the Dynix operating system implemented by Sequent Computer Systems, as explicitly described in col. 6, lines 7 - 10. This is a symmetrical multiprocessing (SMP)

architecture similar to the Sequent Computer system described on page 6 of Applicant's specification [models S2000/450, S2000/750].

As per claims 12, 25:
Spix teaches a parallel processing system [col. 7, line 48].

As per claims 13, 26:
Spix teaches a loosely coupled distributed processing system which uses the Amoeba operating system [col. 5, lines 51, 52].

Claims 2, 3, 16, 17, 27 and 28 are rejected under 35 U.S.C. § 103 as being unpatentable over Spix et al. (U.S. Patent 5,179,702, issued Jan. 12, 1993) in view of Record et al. (U.S. Patent 5,305,454, issued Apr. 19, 1994, filed Aug. 12, 1991), and further in view of Hillis (U.S. Patent 5,303,297, issued Apr. 12, 1994, filed Jul. 25, 1991).

As per claims 2, 3, and 27:
Spix & Record disclose the invention substantially as claimed, as discussed above and further expanded below:

> *Spix teaches a symmetric multiprocessing computer system which uses the Dynix operating system implemented by Sequent Computer Systems, as explicitly described in col. 6, lines 7 - 10.*
> *Spix teaches a plurality of processors sharing a single copy of an operating system with each of the processors configured to execute a single process at any one time and each of the processors having read and write access to a least one common memory [abstract, col. 6, lines 7 - 10, col. 7, lines 46 - 59]. Spix teaches at least one disk drive which inherently communicates with a system bus through an I/O controller with each of the processors and at*

least one common memory [fig. 2]. Spix teaches run queue means coupled to the processors for holding a sequential list of "segments" (i.e., jobs or tasks) to be processed [fig. 1b, 4a, 4b]. Spix teaches process creation means and distributing means for distributing the jobs (i.e., "discrete events") [cols. 1, 2, fig. 6b].

However, **Spix & Record** do not explicitly disclose a system for processing customer billing and invoice jobs.

Hillis discloses a system for processing customer billing and invoice jobs in the analogous field of endeavor of real time processing
for the purpose of providing a system which efficiently processes large numbers of customer bills and invoices and has the additional feature of delivering the billing information to the subscriber in real time [col. 5, line 39, fig. 2: billing computer 32, abstract].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to improve upon the multi processor scheduler and event handler as taught by **Spix & Record** by implementing a system for processing customer billing because it would provide **Spix & Record's** system with the enhanced capability of efficiently processing large numbers of customer bills and invoices.

As per claim 16:
Hillis discloses a system for processing customer billing which uses a customer account which is tracked in real time, as detailed above in the rejection of claim 14 [abstract, col. 6].

As per claim 17:

Hillis discloses a system for processing a customer account (i.e., "a discrete event") which is tracked in real time, as detailed above in the rejection of claim 14 [abstract, col. 6].

As per claim 28:

Spix teaches that a plurality of segments (i.e., "process queues") are initiated to execute concurrently on at least one processor [col. 9, lines 10 - 15]. Spix teaches that each independent "sub-event" (i.e., "thread") is processed sequentially as determined by priority [col. 9, lines 19 - 23]. It is inherent that the results of the processing are stored. Spix teaches a highly parallel multi processor system having multiple tightly-coupled processors that share a common memory which stores "discrete events" (i.e., processes and/or threads).

Conclusions

Claims 8, 9, 22 and 23 appear to be allowable over the prior art of record which does not teach or suggest the combined recited steps of: dividing the number of discrete events by the number of segments to determine a segment size and a remainder; selecting a number of segments equal to the remainder; and distributing sequentially into each segment a number of discrete events equal to the segment size for each segment.

Requested Format of Amended Claims:

Please help expedite the prosecution of this application by including the text of all claims which remain in the case in your amendment response. Please label each amended claim as (AMENDED) after the claim number. Please label each unchanged claim (UNCHANGED) after the claim number. Please label each canceled claim (CANCELED) after the claim number. The text of a canceled claim does not need to be included. Please include line numbers in the left margin on each page that contains claims. This format is not mandatory, however, it will help expedite the processing of your application. Your cooperation is appreciated.

THIS ACTION IS MADE FINAL.

Applicant is reminded of the extension of time policy as set forth in 37 C.F.R. § 1.136(a).

A SHORTENED STATUTORY PERIOD FOR RESPONSE TO THIS FINAL ACTION IS SET TO EXPIRE THREE MONTHS FROM THE DATE OF THIS ACTION. IN THE EVENT A FIRST RESPONSE IS FILED WITHIN TWO MONTHS OF THE MAILING DATE OF THIS FINAL ACTION AND THE ADVISORY ACTION IS NOT MAILED UNTIL AFTER THE END OF THE THREE-MONTH SHORTENED STATUTORY PERIOD, THEN THE SHORTENED STATUTORY PERIOD WILL EXPIRE ON THE DATE THE ADVISORY ACTION IS MAILED, AND ANY EXTENSION FEE PURSUANT TO 37 C.F.R. § 1.136(a) WILL BE CALCULATED FROM THE MAILING DATE OF THE ADVISORY ACTION. IN NO EVENT WILL THE STATUTORY PERIOD FOR RESPONSE EXPIRE LATER THAN SIX MONTHS FROM THE DATE OF THIS FINAL ACTION.

How to Contact the Examiner:

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to **St. John Courtenay III** whose telephone number is **(703) 308-5217.**

Please send all FAX transmissions to **(703) 308-5359.**

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is **(703) 305-9600.**

ST.JC/ST.JC 8-27-96

KEVIN A. KRIESS
PRIMARY EXAMINER
GROUP 2300